13 have been amended, Claims 14-20 have been cancelled and Claims 21-32 have been added by the present amendment.

In the outstanding Office Action, the drawings were objected to; the claims were objected to because they include reference characters which are not enclosed within parentheses; the title of the invention was objected to; Claims 3-5 and 8 were rejected under 35 U.S.C. § 112, second paragraph; Claims 1-11 and 13 were rejected under 35 U.S.C. § 103(a) as unpatentable over Takahashi (U.S. Pat. No. 5,960,264, hereafter Takahashi '264) in view of the same named Takahashi (U.S. Pat. No. 6,001,678, hereafter Takahashi '678); and Claim 12 was rejected under 35 U.S.C. § 103(a) as unpatentable over Takahashi '264 in view of Takahashi '678 and Uenishi et al (U.S. Pat. No. 5,894,149).

In response to the objection to the drawings, Figures 27 and 28 are being labeled "PRIOR ART" as requested in the outstanding Office Action. A separate Letter Requesting Approval requesting approval of these changes is being submitted to the Draftsman. Accordingly, it is respectfully requested this objection be withdrawn.

Regarding the objection of the claims, the claims have been amended to omit all reference characters. Accordingly, it is respectfully requested this objection be withdrawn.

Regarding the objection of the title, a new title has been added that is clearly indicative of the invention to which the claims are directed. Accordingly, it is respectfully requested this objection be withdrawn.

In response to the rejection of Claims 3-5 and 8 under 35 U.S.C. § 112, second paragraph, Claims 3-5 and 8 have been amended in light of the comments noted in the outstanding Office Action and as shown in the marked-up copy. Claims 3-5 and 8 have not been amended to overcome any cited art. No new matter has been added. Accordingly, it is respectfully requested this rejection be withdrawn.

The Abstract has been amended to remove references to figures and to correct minor informalities. No new matter has been added.

Turning to the rejection on the merits, Claim 1 has been amended to more clearly recite the present invention and finds support in Figure 1.

Amended Claim 1 is directed to a semiconductor device having a first semiconductor layer, a second semiconductor layer, a third semiconductor layer, a fourth semiconductor layer, at least one first trench and at least one second trench. A first semiconductor region is selectively formed in a surface of the fourth semiconductor layer, vicinal to the at least one first trench. A first material serving as a control electrode is buried in the at least one first trench and a second material is formed in the at lest one second trench and is not a control electrode. Further, a first main electrode is electrically connected to the second material formed in the at least one second trench and the first main electrode is formed over a surface of the fourth semiconductor layer.

In a non-limiting example, Figure 1 shows the first semiconductor layer 1, the second semiconductor layer 3, the third semiconductor layer 4, the fourth semiconductor layer 5, the at least one first trench 7 and the at least one second trench 11. The first semiconductor region 6 is formed vicinal to the at least one first trench 7 and the first material 9 is buried in the at least one first trench 7 and serves as the control electrode. The second material 15 is formed in the at least one second trench 11 and is electrically connected to the first main electrode 12. By virtue of being connected to the first main electrode 12, the second material 15 is incapable of performing a control function, and thus no control electrode is provided in the second trench.

The semiconductor device of the present invention, by having the at least one second trench functioning as a dummy trench, advantageously achieves a large contact area between

an emitter electrode 12 and the P base layer 5 without decreasing a breakdown voltage and increasing an ON-state voltage.[1]

In addition, by forming the second trench between first trenches as showed in Figure 1, the semiconductor device achieves a decreased gate capacity, a reduced ON-state voltage, and no breakdown voltage drop. Figure 30 of the present specification shows that reducing the gate electrode to decrease the gate capacity in an element structure shown in Figure 28, results in a dropping of the breakdown voltage although a trench space is increased and the gate capacity is decreased (LC curve in Figure 30). The drop in the breakdown voltage depends on a carrier concentration of an N^- layer and a trench depth. The drop in the breakdown voltage becomes pronounced because of the presence of the N layer 34 in Figure 28. To prevent such breakdown voltage drop, the second trench 15 is formed as shown in Figure 1. Also, by forming the second trench 15, a space between first trenches 10 becomes larger compared to the case where the second trench is not formed. A problem in a conventional structure shown in Figure 28 is that having merely an N layer 34, the breakdown voltage is low, as shown in Figure 30, although it is possible to decrease the gate capacity due to the presence of the N layer 34. However, with the structure of the present invention is possible to obtain a semiconductor device having an excellent element characteristic in which the gate capacity is decreased and the breakdown voltage is high.

Takahashi '264 discloses a semiconductor device having a control electrode 49 in each trench, as shown in Figure 3. However, Takahashi '264 does not teach or suggest a second

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[1]Specification, page 22, line 25, to page 23, line 16.

material formed in at least one second trench connected to a first main electrode, and therefore each and every material formed in the trench in Takahashi '264 is a control electrode, as recognized in the outstanding Office Action at page 4, last two lines.

Takahashi '678 discloses in Figure 9 an intermediate step of a method for producing an insulated gate semiconductor device, and the final product of this method is shown in Figure 12. Therefore, Applicant respectfully submits the incomplete device shown in Figure 9 is inoperable as an insulated gate semiconductor device as claimed. It is therefore meaningless to compare the incomplete inoperable device of Takahashi '678 with the completed operable claimed device of the present invention.

Furthermore, assuming arguendo that a comparison with Figure 9 of Takahashi '678 were appropriate, the incomplete device shown in Figure 9 of Takahashi '678 has a plurality of trenches 68, *each trench* having a vicinal N^+ region 66, an N layer 63 and a channel region 64 formed between the region 66 and the layer 63. Thus, there is no distinction among the structures of the trenches 68 in Takahashi '678, and clearly it would be without basis in the Takahashi '678 reference to assume any difference in structure or functionality in the plural trenches 68, contrary to the claimed invention.

Note that in the intermediary Figure 9 illustration there is no first main electrode and there is no disclosure of electrical connections of the material 70 in trenches 68 to the first main electrode, or any other electrode. The final product shown in Figure 12 is an insulated gate bipolar transistor[2] (IGBT), the same type of device disclosed in Takahashi '264. As stated in the outstanding Office Action, at page 4, item 10, Takahashi '264 uses the material 49 (which corresponds to material 70 in Takahashi '678) as a control electrode. Therefore, the material 70 must be the control electrode in Takahashi '678, in each trench 68.

Reiterating, it is inconsistent and improper to pick one trench of the incomplete device in Figure 9 in Takahashi '678 and to distinguish that trench over the remaining *identical* trenches in Figure 9 when all of the trenches have an identical structure. In addition, none of the materials formed in any trench in Takahashi '678 is electrically connected to the first main electrode. Accordingly, Applicant respectfully submits Takahashi '678 does not teach or suggest a semiconductor device having a second material connected to the first main electrode that is not a control electrode, formed in at least one second trench.

Thus, the combination of Takahashi '264 and Takahashi '678 fails to teach every element of the claimed invention. Accordingly, Applicant respectfully submits amended Claim 1 and the claims depending therefrom patentably distinguish over Takahashi '264 in view of Takahashi '678.

Regarding the rejection of Claim 12 under 35 U.S.C. § 103(a) as unpatentable over Takahashi '264 in view of Takahashi '678 and Uenishi et al, the outstanding Office Action asserts Uenishi et al. for the teaching of an electrode 10 formed on a conductive region 80, in Figure 42.[3] However, Uenishi et al do not teach or suggest what is also lacking in Takahashi '264 and Takahashi '678, namely, a material formed in a trench that is not a control electrode and the material in the trench electrically connected to a first main electrode.

Therefore, it is respectfully submitted that no matter how the applied references are combined, the combination fails to teach or suggest the invention defined by Claim 1 and dependent Claim 12.

New Claims 21-32 have been added to set forth the invention in a varying scope. In particular, Claims 21-32 depend directly or indirectly on independent Claim 1 and find

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[2] Takahashi '678, column 14, lines 45-49.

[3] Outstanding Office Action, page 7, last paragraph.

support in Figure 1.

In more detail, Claim 21 further states structure clearly differentiating over Figure 9 of Takahashi '678 which shows that the first semiconductor region 66 is vicinal to each trench 68, whether the trench is of a first or second trench type. Claim 22 is dependent on Claim 21 and recites the first main electrode is formed in direct contact over the entire top surface of the fourth semiconductor layer around the at least second trench. This feature further distinguishes the claimed invention over the applied art because in the applied art a top surface of the fourth semiconductor layer is mainly covered by a first semiconductor region and not by the first main electrode. Claim 23 depends on Claim 22 and recites the first main electrode is formed in direct contact over the entire top surface of the fourth semiconductor layer between the at least one first trench and the at least one second trench, contrary to Takahashi '264 in which the first main electrode is not in direct contact to the entire top surface of the fourth semiconductor layer between the trenches.

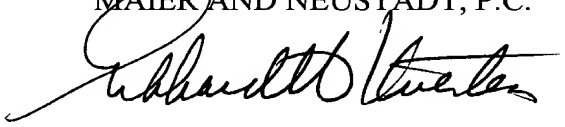
Claim 24 recites a plurality of first trenches and at least one second trench being provided between two adjacent first trenches. Claim 25 is dependent on Claim 24 and further recites a plurality of second trenches. As discussed above, none of the applied art teaches or discloses a second trench not having a control electrode and connected as claimed.

Further, new Claims 26, 28 and 30 are similar to Claim 22 and new Claims 27, 29 and 31 are similar to Claim 23, but have different dependencies. In addition, Claim 32 recites that the first material is identical to the second material. Accordingly, it is respectfully submitted new Claims 21-32 are allowable for similar reasons as discussed above.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER AND NEUSTADT, P.C.



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Marked-Up Copy

Serial No: 09/986,277
Amendment Filed on: December 11, 2002

IN THE TITLE

Page 1, line 2, delete in its entirety and substitute therefor:

SEMICONDUCTOR DEVICE HAVING FIRST AND SECOND TRENCHES WITH NO CONTROL ELECTRODE FORMED IN THE SECOND TRENCH [SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME]

IN THE CLAIMS

Please amend the claims as follows:

--1. (Amended) A semiconductor device comprising:

a first semiconductor layer [1] of a first conductivity type having first and second major [surface] surfaces;

a second semiconductor layer [3] of a second conductivity type formed on the first major surface of said first semiconductor layer;

a third semiconductor layer [4] of the second conductivity type formed on said second semiconductor layer;

a fourth semiconductor layer [5] of the first conductivity type formed on said third semiconductor layer;

[a] at least one first trench and at least one second trench [7, 11] arranged to penetrate through at least said fourth semiconductor layer from a surface of said fourth semiconductor

layer;

a first semiconductor region [6] of the second conductivity type selectively formed in said surface of said fourth semiconductor layer [adjacently] vicinal to said at least one first trench;

a first insulating film [8] formed on an internal wall of said at least one first trench;

a first material serving as a control electrode [9] buried in said at least one first trench [through] and formed on said first insulating film[, said control electrode being not formed in said at least one second trench];

a second material formed in said at least one second trench, the second material not being a control electrode;

a first main electrode [12] electrically connected to said second material formed in said at least one second trench and to at least a part of said first semiconductor region and formed over [an almost whole] a surface of said fourth semiconductor layer; and

a second main electrode [13] formed on the second major surface of said first semiconductor layer.

2. (Amended) The semiconductor device according to claim 1, wherein

a distance between said at least one first trench and said at least one second trench is [set to] 5 μm or less.

3. (Amended) The semiconductor device according to claim 1, wherein

said at least one first trench includes a trench formed in a predetermined direction [seen on a plane] along said first major surface of said first semiconductor layer,

said at least one second trench includes a trench formed in said predetermined direction [seen on a plane],

said first semiconductor region includes a first [partial region] section formed in [the]

a vicinity of said at least one first trench and a second [partial region 6a to 6c] section extended from said first [partial region] section in such a direction as to go away from said at least one first trench[;], and

said first main electrode is directly formed on said second [partial region] section to carry out an electrical connection to said first semiconductor region.

4. (Amended) The semiconductor device according to claim 3, wherein

said first semiconductor region includes a third [partial region 6b, 6c] section which is further extended from said second [partial region] section and is formed in [the] a vicinity of said at least one second trench, and

said first main electrode is further formed directly on said third [partial region] section to carry out said electrical connection to said first semiconductor region.

5. (Amended) The semiconductor device according to claim 4, wherein said second and third [partial regions] sections include a plurality of second and third [partial regions] sections respectively, and

said plurality of third [partial regions 6c] sections are selectively formed in the vicinity of said at least one second trench.

6. (Amended) The semiconductor device according to claim 1, further comprising:

a second semiconductor region [16] of the first conductivity type formed in said surface of said fourth semiconductor layer [adjacently] contiguous to said at least one second trench, said second semiconductor region having a concentration of an impurity of the first conductivity type set to be higher than that of said fourth semiconductor layer.

8. (Amended) The semiconductor device according to claim 1, [wherein] further comprising:

[said at least one second trench includes] a plurality of second trenches.

9. (Amended) The semiconductor device according to claim 1, wherein

said at least one first trench and said at least one second trench have equal formation widths.

10. (Amended) The semiconductor device according to claim 1, further comprising:

a second insulating film [14] formed on an internal wall of said at least one second trench.

11. (Amended) The semiconductor device according to claim 10, further comprising [is] a conductive region [15] buried in said at least one second trench [through] and formed on said second insulating film.

13. (Amended) The semiconductor device according to claim 1, further comprising:

a sixth semiconductor layer [2] of the second conductivity type formed between said first semiconductor layer and said second semiconductor layer, said sixth semiconductor layer having a concentration of an impurity of the second conductivity type [set to be] higher than that of said second semiconductor layer.

14-20. (Cancelled).

21-32. (New).--

IN THE ABSTRACT

Page 41, lines 2-15, please amend the Abstract to read as follows:

[It is an object to obtain a] A semiconductor device capable of minimizing an increase in a gate capacity without adversely influencing an operation characteristic and a method of manufacturing the semiconductor device. A first trench [(7)] and a second trench [(11)] are formed to reach an upper layer portion of an N^- layer [(3)] through a P base layer [(5)] and an N layer [(4)], respectively. [In this case, a] A predetermined number of second trenches

[(11)] are formed between [the] first trenches [(7) and (7)]. The first trench [(7)] is provided [adjacently] vicinal to an N^+ emitter region [(6)] and has a gate electrode [(9)] formed therein. The second trench [(11)] has a polysilicon region [(15)] formed therein. The second trench [(11)] is different from the first trench [(7)] in that the N^+ emitter region [(6)] is not formed in a vicinal region [and] of the second trench and the gate electrode [(9)] is not formed therein. A trench space between the first trench [(7)] and the second trench [(11)] which are provided adjacently to each other is set to [be such a distance as] not [to] reduce a breakdown voltage. An emitter electrode [(12)] is directly formed on an almost whole surface of a base region [(5)].